Merchant Silicon Throughput Processing Capacity - Hardware Deep-Dive and Forwarding Engine Specification

MERCHANT SILICON THROUGHPUT PROCESSING CAPACITY - HARDWARE DEEP-DIVE AND FORWARDING ENGINE SPECIFICATION

EXECUTIVE SUMMARY

This document provides a comprehensive technical evaluation of the Next-Generation Merchant Silicon Throughput Processing Engine (MSTP-Series). Designed for high-density data center spine-leaf, carrier PE routers, and campus core deployments, this platform leverages best-in-class merchant switching silicon to deliver non-blocking, line-rate Layer 2/3 forwarding. The architecture decouples control plane software complexity from deterministic hardware forwarding, ensuring predictable sub-microsecond latency and wire-speed processing across all port densities.



HARDWARE ARCHITECTURE & SILICON

The MSTP-Series forwarding engine is built around a centralized or distributed (depending on SKU) merchant silicon fabric. The core silicon integrates a fully shared packet buffer, a ternary content-addressable memory (TCAM) for ACLs and routing lookups, and a high-speed SerDes interconnect. The device eliminates oversubscription in the fabric-to-port mapping, guaranteeing full-duplex throughput on every active interface simultaneously.

KEY FEATURES & ROUTING LOGIC

- Non-Blocking Fabric: Full wire-speed forwarding with zero packet loss under bi-directional 100% line-rate traffic.

- Programmable Pipeline: Supports VXLAN, NVGRE, MPLS, and segment routing termination/encapsulation in hardware.

- Intelligent Buffer Management: Dynamic packet buffer allocation with per-port head-of-line blocking prevention.

- Low Latency: Cut-through switching mode with port-to-port latency below 600ns (for 100G interfaces).

- Flow Processing: Hardware-based hashing for ECMP, link aggregation (LAG), and load balancing.

COMPLIANCE & STANDARDS

The MSTP-series merchant silicon engine adheres to IEEE 802.1Q, 802.1ad (Q-in-Q), 802.3x flow control, and RFC 2544 benchmarking standards. It complies with RoHS, REACH, and FCC/CE emission limits. Forwarding plane security includes hardware MACsec (802.1AE) and IPv6 RA guard.

TECHNICAL SPECIFICATIONS

Parameter	**Specification**
Form Factor	1RU Fixed / 5RU Modular Chassis (SKU dependent)
Switching Capacity	4 Tbps - 128 Tbps non-blocking
Forwarding Rate	Up to 8.4 Bpps (billion packets per second)
MAC Address Table Size	288K entries

IPv4/IPv6 Routes (FIB)	2M / 1M routes
Packet Buffer	32 MB shared, dynamic allocation
Power Supply	Dual hot-swappable AC/DC (1+1 redundancy)
Typical / Max Power	180W / 280W (1RU variant)
Latency (64-byte)	Sub-600ns (100G ports)

ORDERING INFORMATION

- MSTP-48YS: 48x 25GbE SFP28 + 8x 100GbE QSFP28, 4 Tbps switching capacity.

- MSTP-32D: 32x 400GbE QSFP-DD, 25.6 Tbps switching capacity.

- MSTP-FABRIC-128: Distributed chassis fabric module, 128 Tbps backplane.



OPERATIONAL ADVANTAGES

Merchant silicon unlocks deterministic throughput at commodity economics, enabling brownfield upgrades without control plane retraining. The MSTP-series supports telemetry streaming (gNMI), PTP (IEEE 1588v2), and SyncE for 5G xHaul transport.

SUPPORT & LIFECYCLE

Five-year hardware warranty with next-business-day advance replacement. Global technical assistance center (TAC) support 24/7. Software maintenance releases offered for seven years from end-of-sale announcement.

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